

One Day Seminar on

Wireless Architectures, VLSI and Embedded Systems (WAVES-2026)

Reliable Memory Design for Deep Submicron VLSI in Radiation Environments

Institution of Engineers
UP State Centre Lucknow
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Er. Shahneela Jamal Kidwai
Research Scholar
A.M.U, Aligarh

Why Radiation Hardening

NASA's Clementine
Mission, 1994



Figure 1: The Clementine engineering model

Need for Radiation Hardened Memory

Space
systems

Small satellites, onboard imaging, autonomy and interplanetary missions all need memory that survives cumulative dose and particle strikes without frequent resets.

Automotive
edge AI

Autonomous vehicles are moving towards the edge for latency and privacy; that increases dependence on local SRAM, caches and parameter memories in safety-critical hardware.

Harsh
environments

Nuclear, avionics, medical and defense electronics increasingly combine advanced nodes with reliability constraints, making soft-error resilience a mainstream design issue.

The Scaling Issue

What scaling improves

- Higher density, lower dynamic power, and larger on-chip memory.
- Faster local data access for processors, AI engines, and mixed-signal control loops.
- Better cost-per-function for complex SoCs and edge devices.

What scaling worsens

- Lower supply voltage and smaller stored charge reduce upset margin.
- Node proximity raises the chance of multi-node charge collection.
- Parametric variation narrows the safe design window under PVT corners.

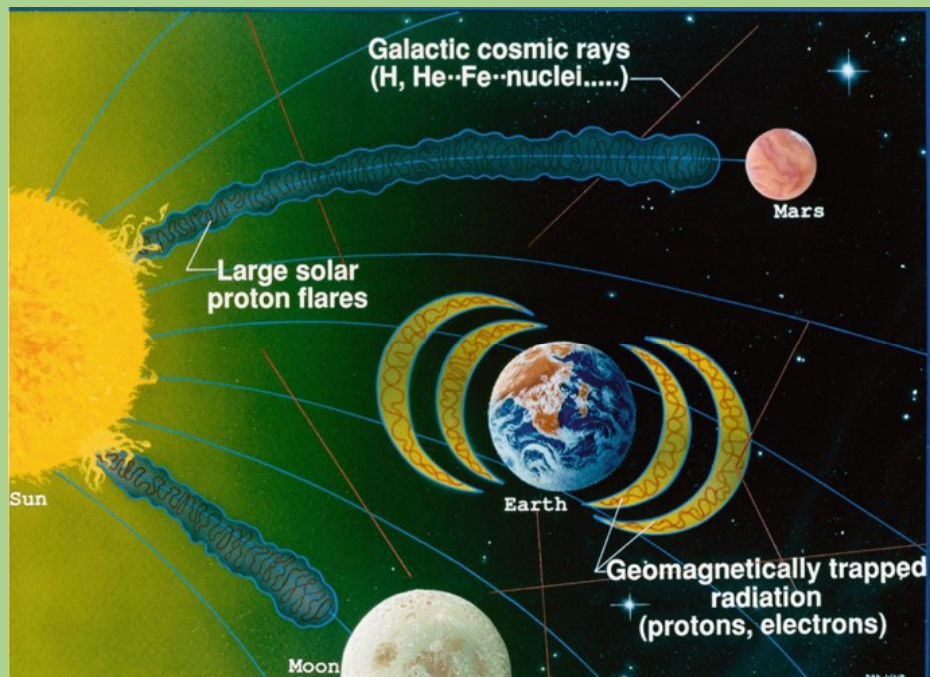


Figure 2: Radiation Sources

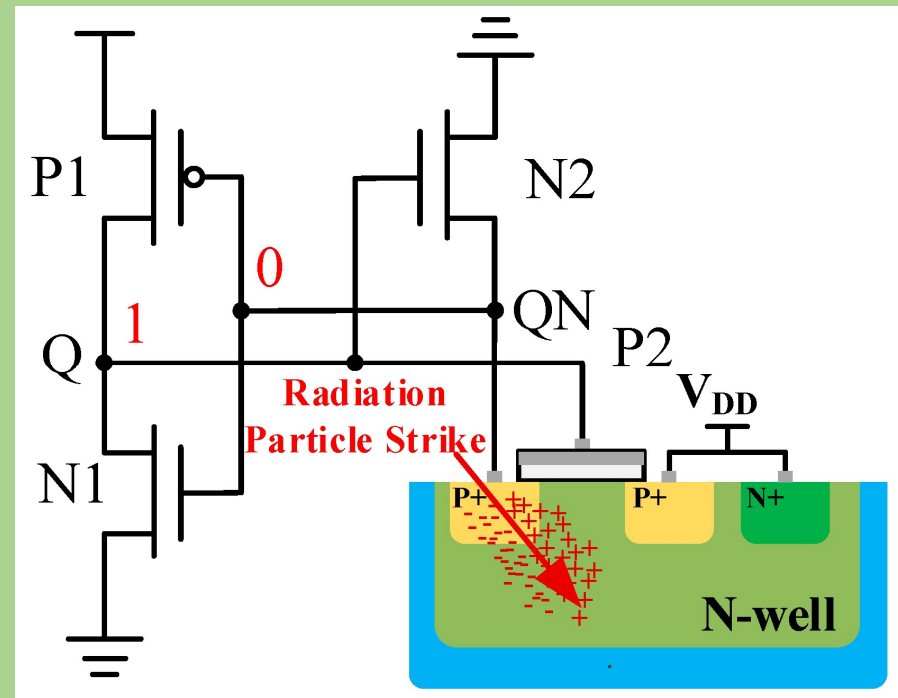


Figure 3: Impact on Electronic Devices

6T SRAM Limitations and Particle strike modelling

- Two cross coupled inverters – only two storage nodes
- No redundancy-no self recovery after upset.
- Highly sensitive to particle strike at storage nodes.
- Poor robustness in scaled technologies.

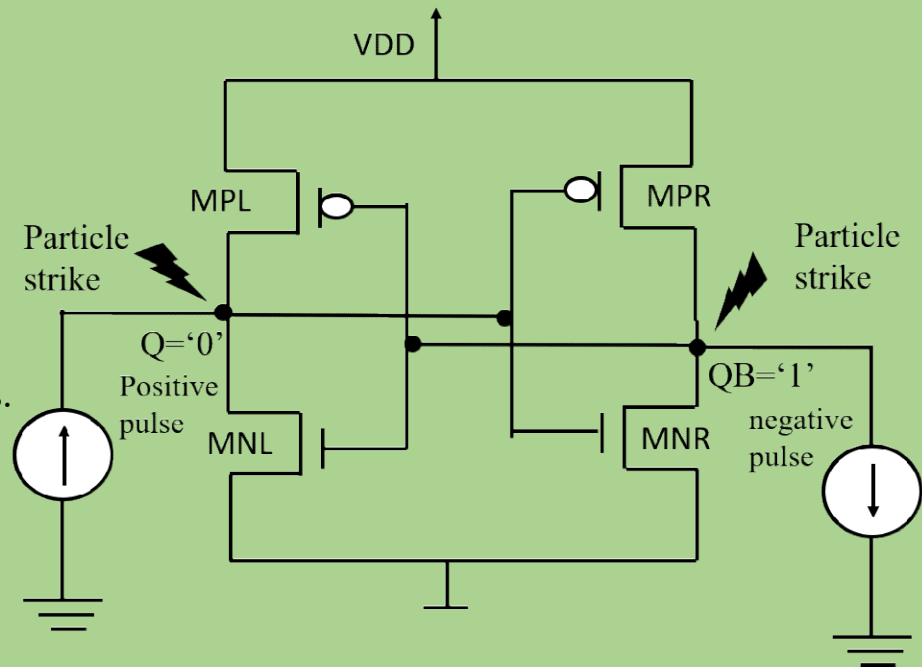


Figure 4: Modelling of particle strike on 6T SRAM cell

Modelling of Injected charge

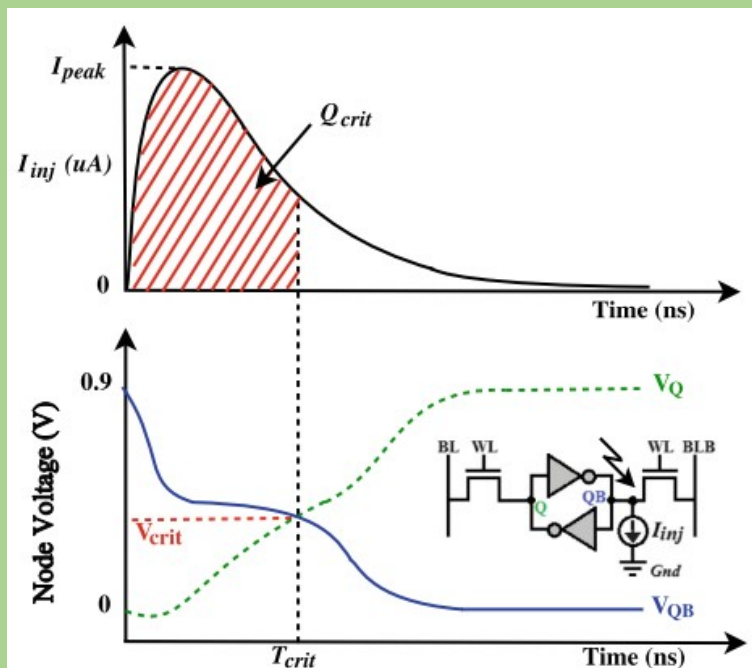


Figure 5(a): Graphical representation defining critical charge.

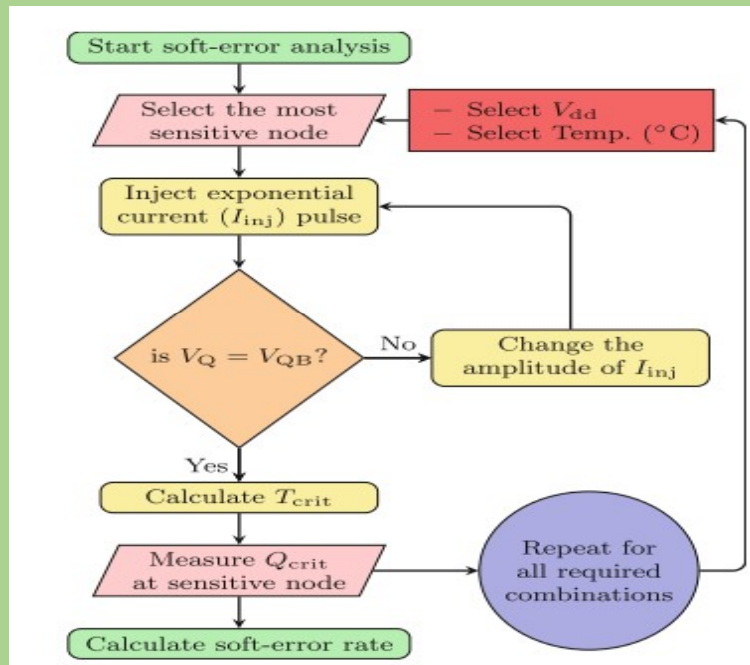


Figure 5(b): Simulation flow of soft-error analysis with different operating temperatures and supply voltages

Types of Radiation Effects

Radiation Effects

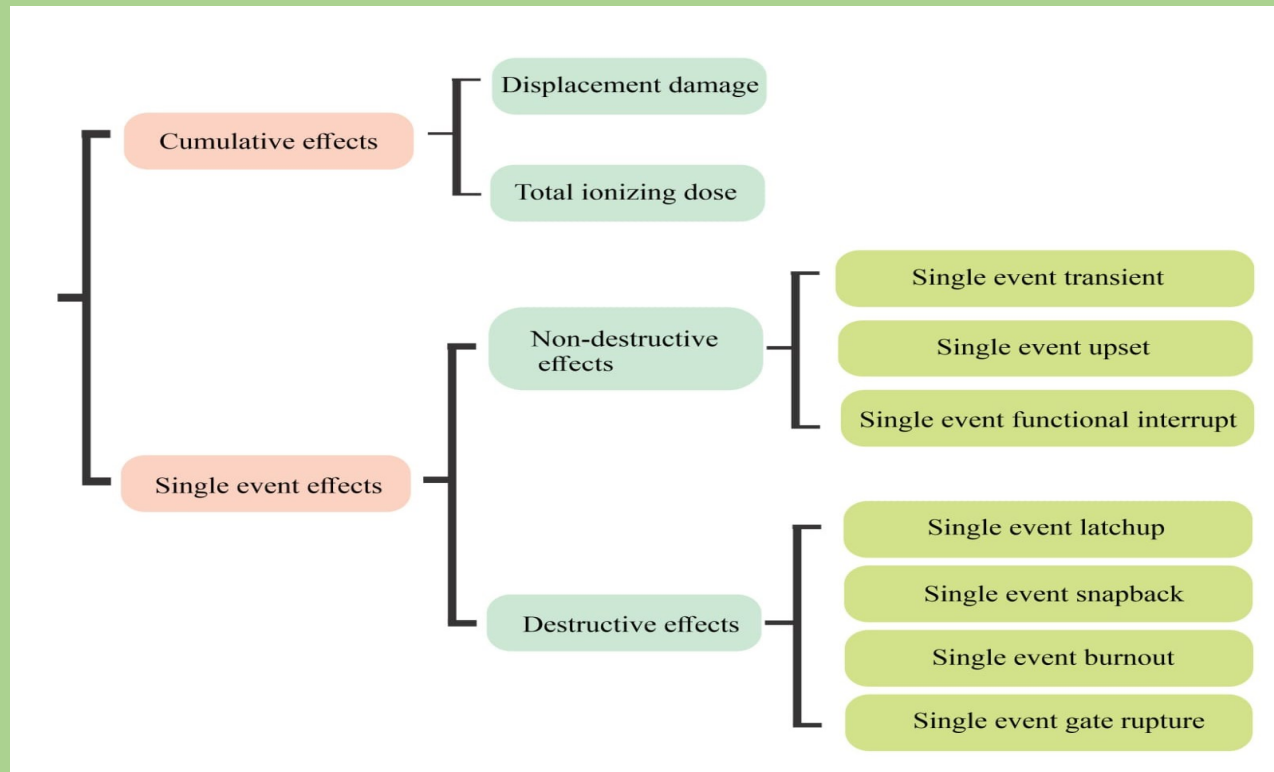


Figure 6 : Types of Radiation Effects

Types of Radiation Effects

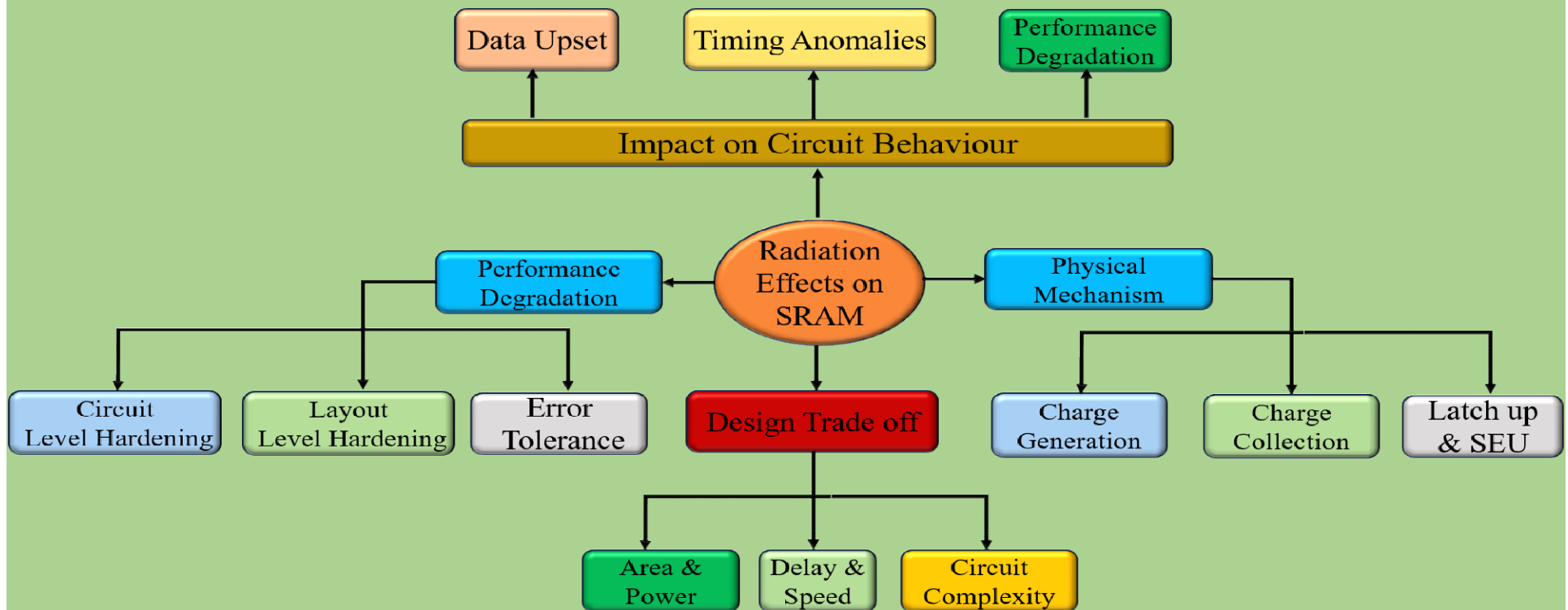


Figure 7: Types of Radiation Effects

From Radiation strike to bit flip

Step 1

An energetic particle deposits charge in silicon, especially at a sensitive storage node or nearby diffusion region.

Step 2

If the collected transient charge exceeds the node's critical charge, the stored state may invert.

Step 3

The upset may remain local, spread to adjacent nodes or propagate upward as corrupted instructions, data, weights, or control bits.

Step 4

At system level, the effect can be a benign glitch, silent data corruption, mission interruption, or unsafe actuation depending on context.

Current scenario examples

LEO satellites

Earth-observation payloads stream large image volumes, so memory upsets can affect buffering, calibration tables, and onboard AI pre-processing during long mission life.

Autonomy

Perception stacks depend on SRAM-rich accelerators and local memory because edge execution cuts latency versus cloud paths and avoids connectivity dependence.

Nuclear electronics

Control electronics near radiation sources need graceful degradation, error detection and hardened memory paths rather than assuming ideal terrestrial conditions.

What gets affected in a modern SoC

L1/L2

Processor caches dominate fast local storage and are frequent soft-error concern points.

SRAM macros

Register files, scratchpads, FIFOs, and packet buffers often outnumber logic by area.

BRAM

FPGA block memories are critical in aerospace and embedded AI deployments.

NVM

MRAM, ReRAM, FeRAM, and advanced NAND are considered for specific harsh-environment roles.

Why SRAM remains central

SRAM still wins where speed, random access, and repeated write activity matter: CPU caches, GPU/AI local memory, temporary state storage and timing-critical control paths.

The challenge is balance: strong upset recovery usually increases transistor count, area, write complexity or power. Good designs target the right trade-off for the application instead of maximizing hardness at any cost.

Design-level hardening options

Cell topology

Use 10T/12T/14T/16T or feedback-based cells that isolate read disturb, separate storage nodes, or enable self-recovery after upset.

Layout strategy

Node spacing, guard structures, interleaving, and careful device placement reduce charge sharing and multi-node upset sensitivity.

System support

ECC, parity, redundancy, and fault-aware software prevent a single cell event from becoming a mission-level failure.

AI hardware adds a new urgency

Embedded DNN platforms for autonomous driving and aerospace are explicitly studied for soft-error robustness because memory perturbations can change model behavior in safety-critical systems.

Recent work also shows that design choices such as activation functions, pruning, and quantization influence resilience, meaning memory reliability now intersects with AI model architecture and deployment flow.

A practical design workflow

1. Classify

Map memories by criticality: cache, control, buffering, model weights, configuration, logging.

2. Harden

Apply cell-level RHBD only where benefit justifies overhead; avoid uniform overdesign.

3. Protect

Add ECC, interleaving, scrubbing, watchdogs, and fault-injection validation.

4. Verify

Check upset recovery, write/read delay, SNM, leakage, area, and PVT robustness at array level.

Radiation Affecting Human Life

Space camera

A flipped calibration coefficient can distort an image product even when the sensor itself is fine.

Autonomous vehicle

A corrupted feature-map buffer can change an AI perception result before software notices the anomaly.

Medical beam system

A transient in control memory is unacceptable unless detection and safe recovery are built in.

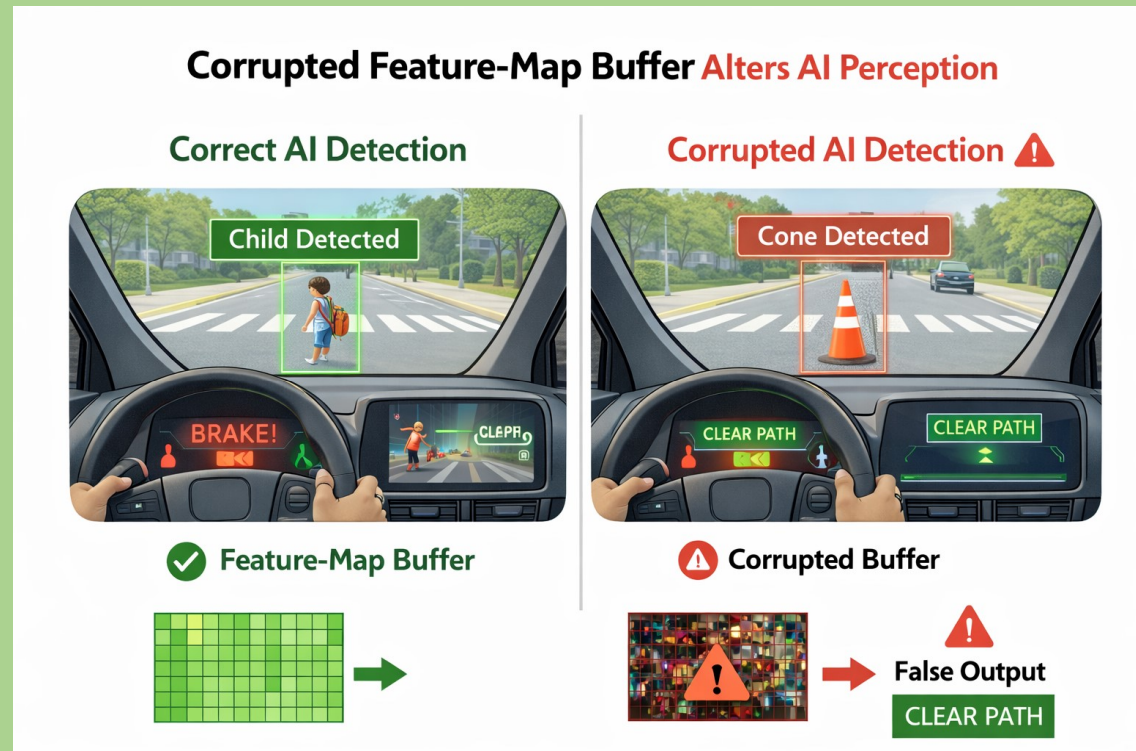


Figure 8: Radiation Affecting Human Life

Conclusion

Advanced scaling improves computing capability but shrinks upset margin.

RHBD SRAM remains essential because fast local memory cannot be replaced everywhere by NVM.

The best 2026 strategy is layered: hardened cells, smart layout, ECC and application-aware architecture.

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Radiation-aware memory design is no longer a niche space-only problem; it is becoming part of mainstream dependable VLSI for edge AI, mobility and harsh-environment electronics.

Thank You!